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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/626,091	07/24/2003	Alaa Y. El-Sherif	TI-35811	4529
7590	04/29/2004			
EXAMINER				
TON, MY TRANG				
			ART UNIT	PAPER NUMBER
			2816	

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DATE MAILED: 04/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/626,091	EL-SHERIF ET AL.	
	Examiner	Art Unit	
	My-Trang N. Ton	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on ____.

2a) This action is **FINAL**. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-26 is/are pending in the application.

4a) Of the above claim(s) ____ is/are withdrawn from consideration.

5) Claim(s) ____ is/are allowed.

6) Claim(s) 1-26 is/are rejected.

7) Claim(s) ____ is/are objected to.

8) Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on ____ is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) All b) Some * c) None of:
1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. ____.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s)/Mail Date. ____ .
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date ____ .	6) <input type="checkbox"/> Other: ____ .

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "third transistor" (claim 6), "the third transistor being an NMOS type" (claim 10) must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

2. The informal drawings filed in this application are acceptable for examination purposes only. When the application is allowed, applicant will be required to submit new formal drawings.

Claim Objections

Claim 14 is objected to because of the following informalities:

In claim 14, last line, after "NMOS", -- . – should be added. Appropriate correction is required.

Abstract

The abstract of the disclosure is objected to because: the clamp circuit (104) does not including "a third transistor (113)" as recited. See Fig. 1. Correction is required. See MPEP § 608.01(b).

Claim Rejections - 35 USC § 112

Claims 1-26 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The description of the present invention in claim 1 is indefinite since it fails to establish the proper structural and/or functional relationship between the recited circuit elements. For example, the limitation "the output of the clamp circuit responsively coupled to the input of the delay circuit" is misdescriptive of the present invention since such limitation is not seen as recited therein. In order to avoid any confusion, Applicant is required to particularly point out how this limitation reads on the circuit arrangement of the drawings. The circuit 101 is referred as "a delay circuit". However, it is not fully clear how and when does "delay" occur.

Claim 6 calls for "the third transistor" which is not seen in the preferred embodiment of the invention. In order to avoid any confusion, Applicant is required to particularly point out how this limitation reads on the circuit arrangement of the drawings. As disclosed in the Abstract, the third transistor is referred to transistor 113. However, Fig. 1 clearly shows the transistor 113 is a part of EEPROM Cell 103. Moreover, the limitation "the gate terminal of the third transistor and the gate of the first transistor being coupled to the second node ..." (lines 14-15). As clearly show in Fig. 1, the gate terminal of the third transistor (113) is connected to RD.

Claim 10 is similarly rejected as claim 6 regarding "the third transistor".

Claim 15 calls for "further comprising a CMOS monolithic integrated circuit" which is not seen in the preferred embodiment of the invention.

Claims 18 and 21 are similarly rejected as claim 1.

Claim 19 is similarly rejected as claim 15.

Claims 2-5, 7-9, 11-14, 16-17, 20, 22-26 are rendered indefinite by the deficiencies of claims above.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-4, 18, 21-22 and 25-26 are rejected under 35 U.S.C. 102(b) as being anticipated by Yach (U.S Patent No. 6,122,205).

Yach discloses in Fig. 1 a voltage regulator and boosting circuit including:
a clamp circuit (12, i.e., 22 is a clamping circuit) with an input (26, 32) and an output (connected between 24, 28);
a delay circuit (14 with delay 33) with an input (connected to 34) and an output (connected to 38);
due to indefinite, the limitation "the output of the clamp circuit responsively coupled to the input of the delay circuit" has not given sufficient weight to read over the reference;

the coupled clamp circuit (12) and the delay circuit (14) operable to keep voltage to one or a plurality of input nodes (node connected to 40) coupling the output of the delay circuit (connected to 38) to a data cell (40, 18, 16) below a predetermined threshold as recited in claim 1.

Regarding claim 2, the delay circuit (14) and the clamp circuit (12) are capable of providing the operation as recited.

Elements 40, 18, 16 read on a data cell as recited in claim 3.

The data cell 40, 18, 16 comprises an EEPROM cell (16) as recited in claim 4.

Claims 18, 21-22 are similarly rejected as above claims 1-4.

The voltage regulator and boosting circuit of Yach is capable of performing the method recited in claims 25-26.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 5, 15-17, 19-20 and 23-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yach as applied to claims 1, 18 and 21 above.

As stated above, every element of the claimed invention recited in above claims can be seen in the circuit of Yach. However, this reference does not show the "predetermined voltage threshold is approximately 10 volts" (claim 5); "CMOS

monolithic integrated circuit" (claims 15, 19, 23); "... for use in a servo motor controller" (claims 16, 20, 24); "... for use in a computer hard drive controller" (claim 17).

Regarding claim 5, although Yach does not expressly state the predetermined voltage threshold is approximately 10 volts, this difference is not of patentable merit because it is notoriously well known in the art that different values for the predetermined voltage threshold can be selected in order to produce correspondingly different output values. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize the predetermined voltage threshold is approximately 10 volts in realizing the circuit of the Yach reference for the purpose of producing different output values when different values of the predetermined voltage threshold is selected.

Regarding "CMOS monolithic integrated circuit", clearly if designer wish to reducing size, reducing cost of manufacture and improving circuit reliability, there is well-known way to do such as: a circuit 10 of Yach can be formed on the integrated circuit.

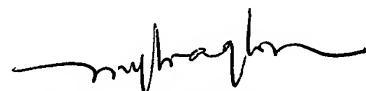
Regarding the limitations "for use in a servo motor controller" or "for use in a computer hard drive controller", it is seen to define an intended use. It would have been obvious to one ordinary skill in the art as routine design expedients know that different type of environments can be selected in order to produce correspondingly different output values.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to My-Trang N. Ton whose telephone number is 571-272-1754. The examiner can normally be reached on 7:00 a.m - 5:30 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



MY-TRANG NUTON
PRIMARY EXAMINER

April 22, 2004